

ABSTRACT

A CMOS bandgap reference (BGR) voltage generator circuit has a passive resistor T-network of low resistance connected between the inverting and non-inverting inputs of the op-amp in the circuit. The op-amp's output is connected to the gates of three PMOS transistors and the drains of two of the transistors are connected in a looped manner to the input terminals of the op-amp. The T-network is placed between these drains that connect to the op-amp. The overall resistance in the present circuit is substantially lower than the resistance in the prior art BGR circuit of comparable performance. Hence, the chip area occupied by the resistors in the circuit is substantially reduced when compared with the area occupied by the resistors in the prior art BGR circuit. The circuit provides a steady reference voltage with sub-1V supply and very low power consumption.